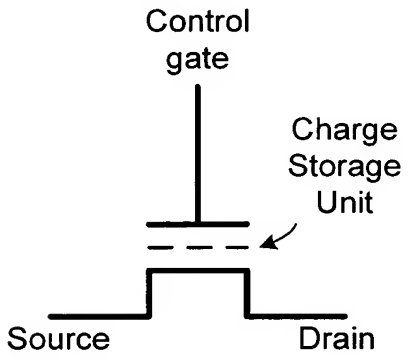

FIG. 1

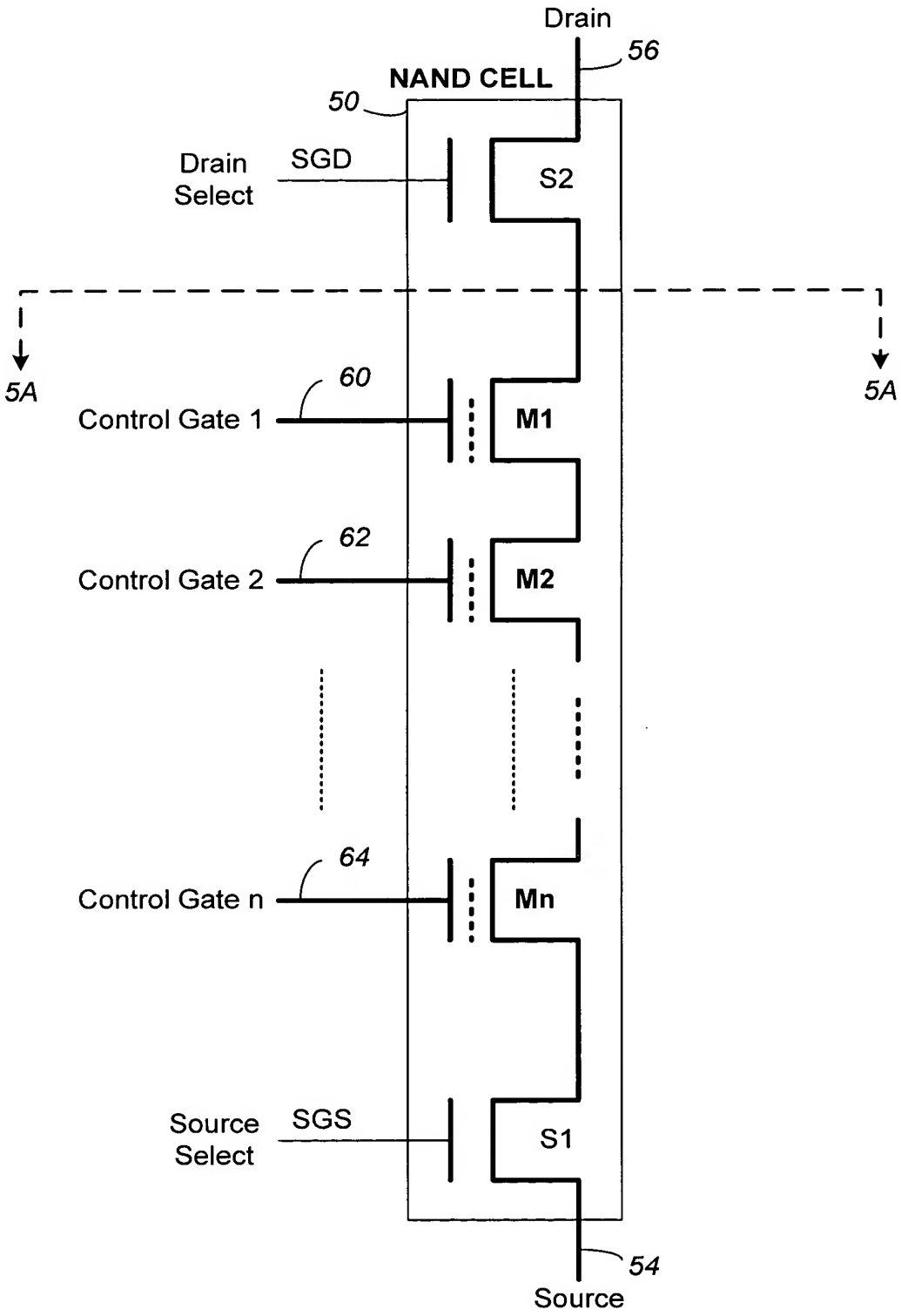
Drain
56
NAND CELL
50
Drain
Select
SGD
S2
5A
5A
60
Control Gate 1
M1
62
Control Gate 2
M2
64
Control Gate n
Mn
Source
Select
SGS
S1
54
Source

FIG. 2

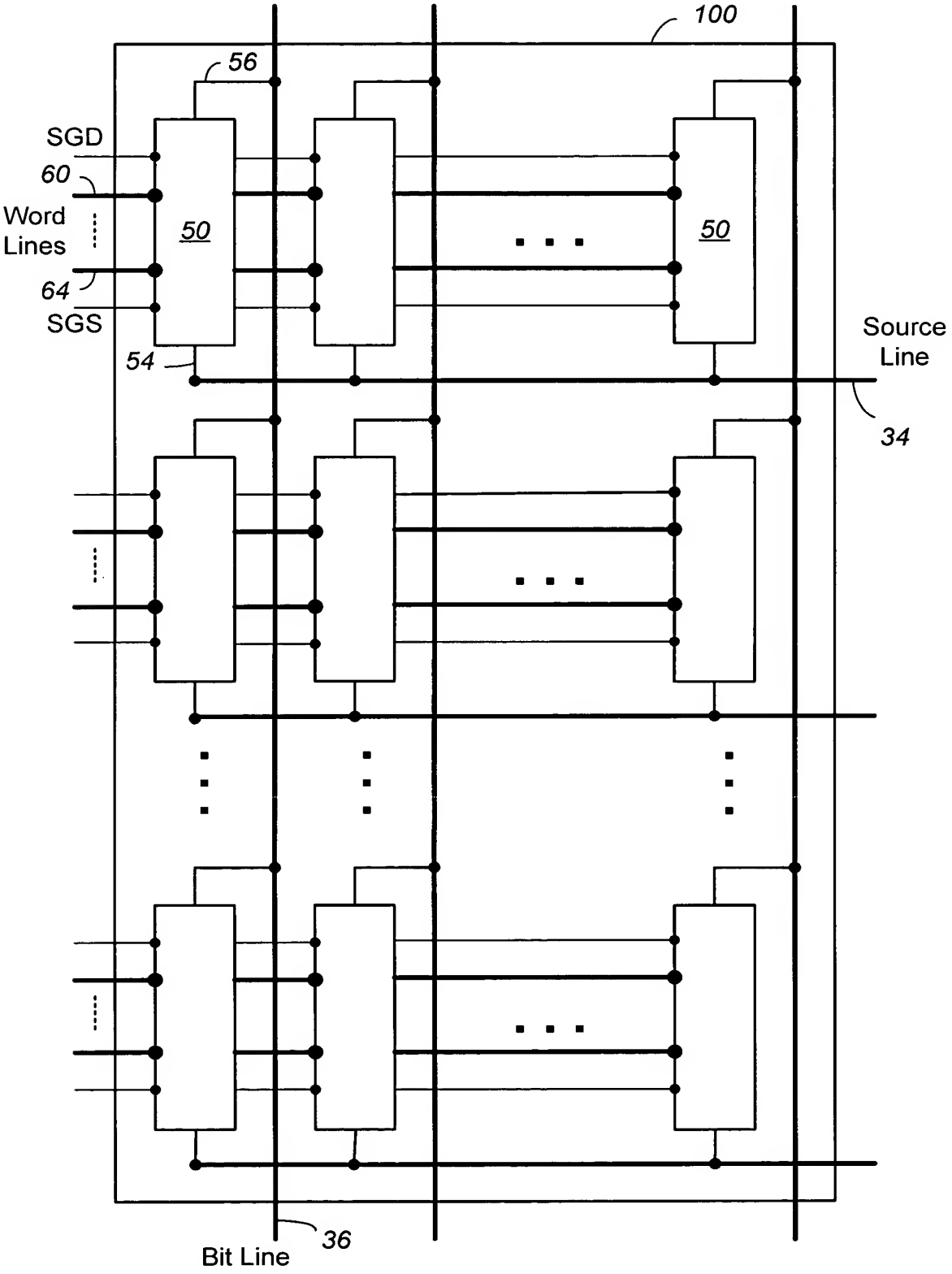
100
56
SGD
60
Word Lines
64
SGS
50
50
54
Source Line
34
36
Bit Line

FIG. 3

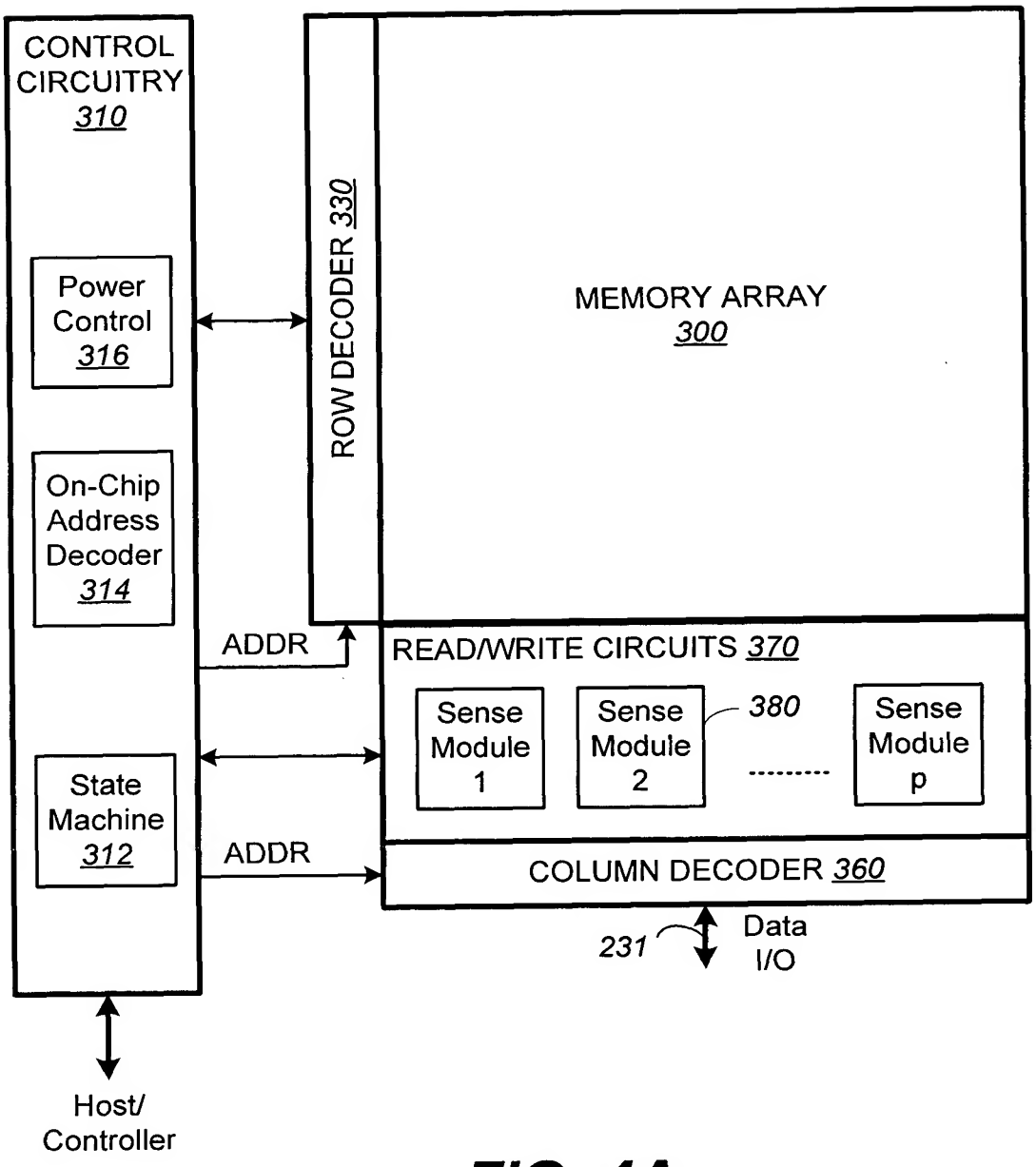
CONTROL CIRCUITRY 310
Power Control 316
On-Chip Address Decoder 314
State Machine 312
ROW DECODER 330
MEMORY ARRAY 300
ADDR
ADDR
READ/WRITE CIRCUITS 370
Sense Module 1
Sense Module 2
380
Sense Module p
COLUMN DECODER 360
231
Data I/O
Host/ Controller

FIG. 4A

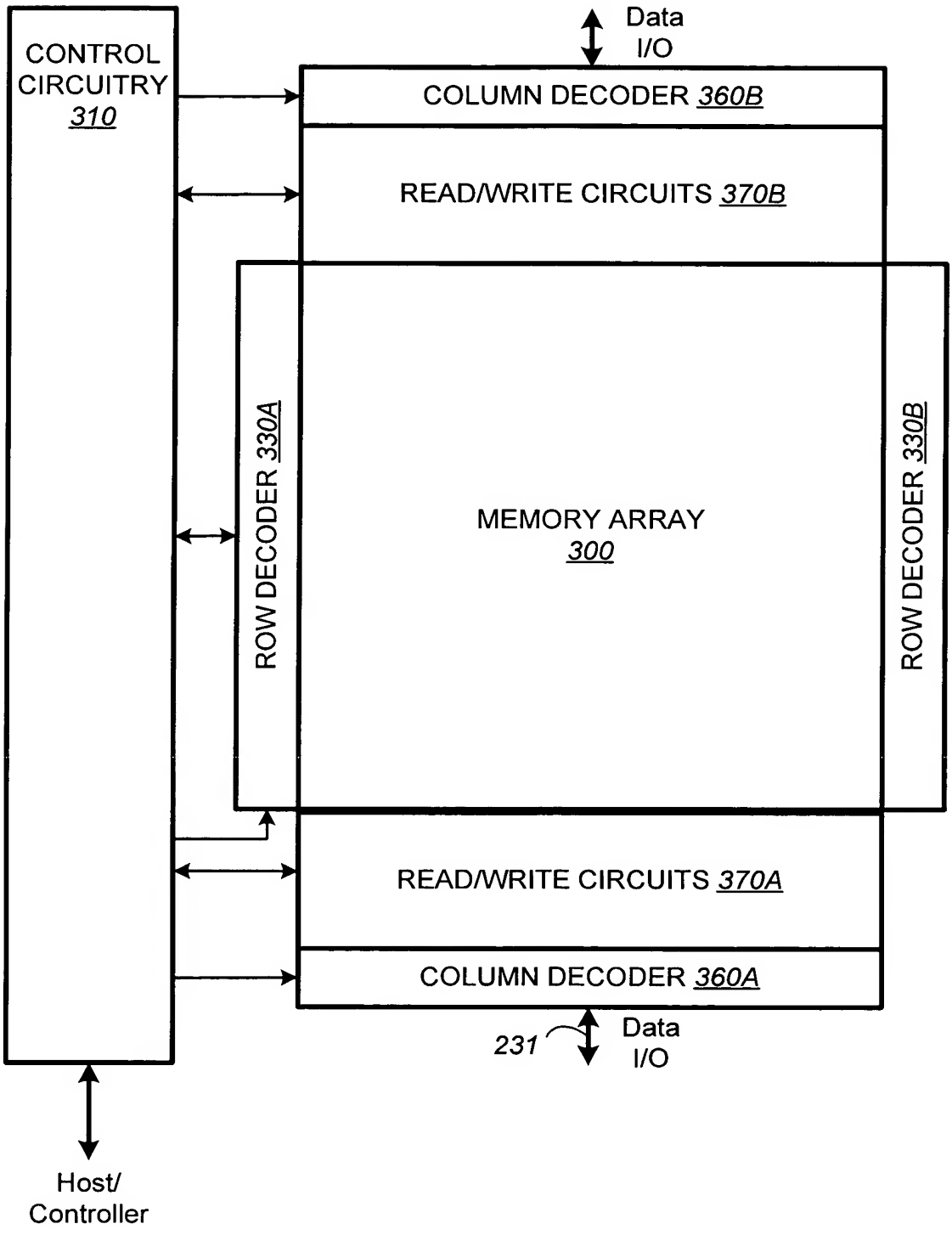
CONTROL CIRCUITRY 310
Data I/O
COLUMN DECODER 360B
READ/WRITE CIRCUITS 370B
ROW DECODER 330A
MEMORY ARRAY 300
ROW DECODER 330B
READ/WRITE CIRCUITS 370A
COLUMN DECODER 360A
231
Data I/O
Host/ Controller

FIG. 4B

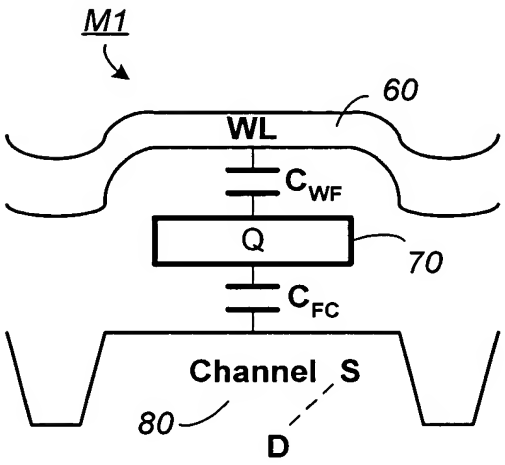
M1
60
WL
C_{WF}
Q
70
C_{FC}
Channel
S
80
D

FIG. 5A

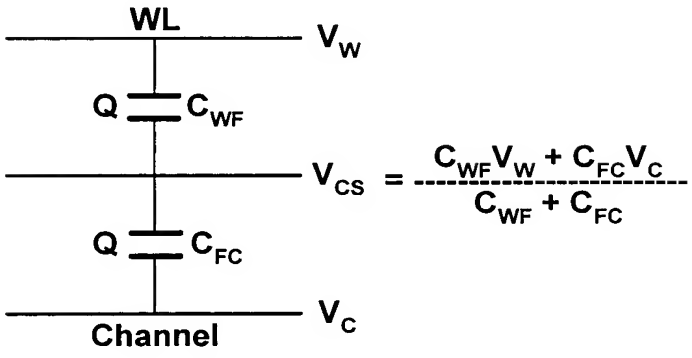
WL
V_W
Q
C_{WF}
$V_{CS} = \frac{C_{WF}V_W + C_{FC}V_C}{C_{WF} + C_{FC}}$
Q
C_{FC}
V_C
Channel

FIG. 5B

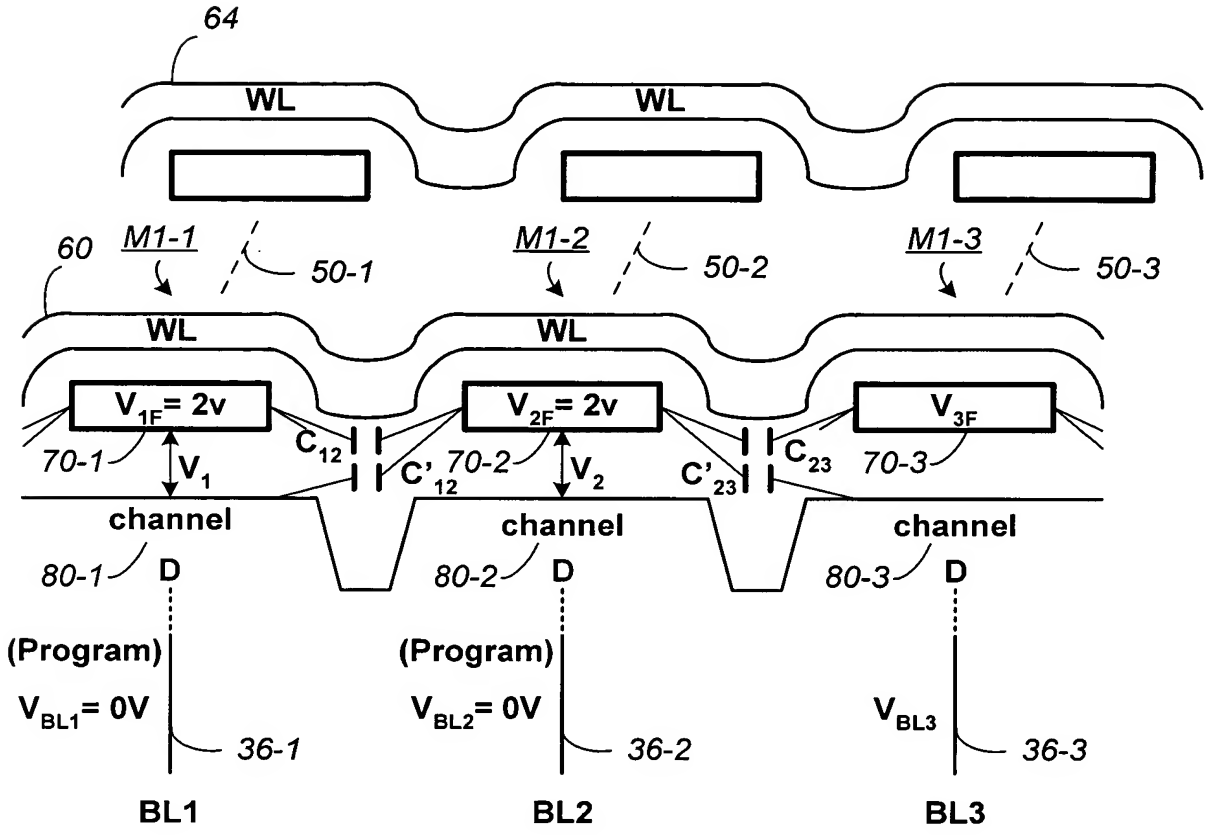
64
WL
WL
60
M1-1
50-1
M1-2
50-2
M1-3
50-3
WL
WL
V_{1F}= 2v
V_{2F}= 2v
V_{3F}
70-1
V_1
C_{12}
C'_{12}
70-2
V_2
C'_{23}
C_{23}
70-3
channel
channel
channel
80-1
D
80-2
D
80-3
D
(Program)
V_{BL1}= 0V
(Program)
V_{BL2}= 0V
V_{BL3}
36-1
36-2
36-3
BL1
BL2
BL3

FIG. 6A

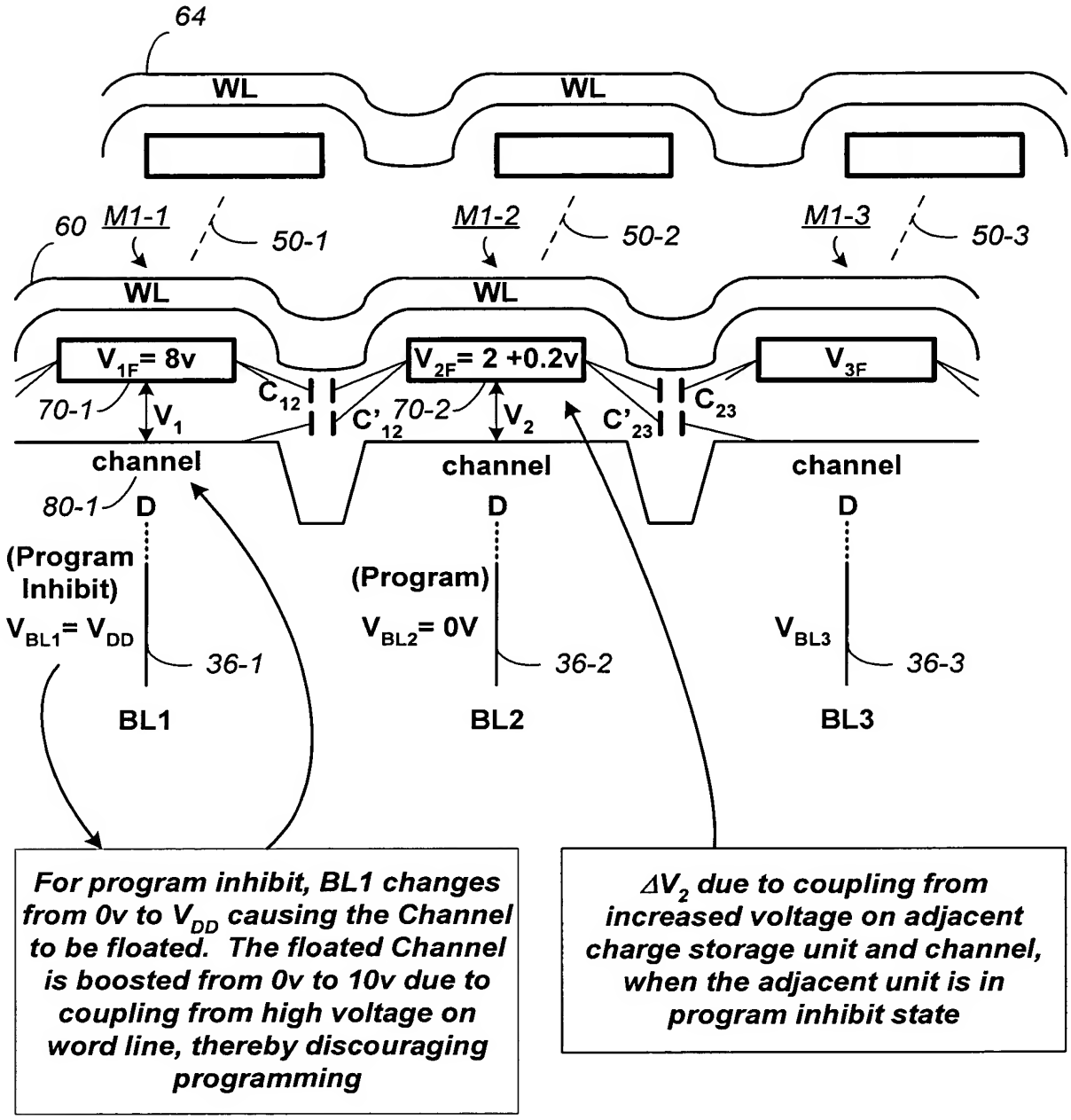
64
WL
WL
60
M1-1
50-1
M1-2
50-2
M1-3
50-3
WL
WL
V_{1F}= 8v
V_{2F}= 2 +0.2v
V_{3F}
70-1
V_1
C_{12}
C'_{12}
70-2
V_2
C'_{23}
C_{23}
channel
channel
channel
80-1
D
D
D
(Program Inhibit)
V_{BL1}= V_{DD}
(Program)
V_{BL2}= 0V
V_{BL3}
36-1
36-2
36-3
BL1
BL2
BL3
For program inhibit, BL1 changes from 0v to V_{DD} causing the Channel to be floated. The floated Channel is boosted from 0v to 10v due to coupling from high voltage on word line, thereby discouraging programming
ΔV_2 due to coupling from increased voltage on adjacent charge storage unit and channel, when the adjacent unit is in program inhibit state

FIG. 6B

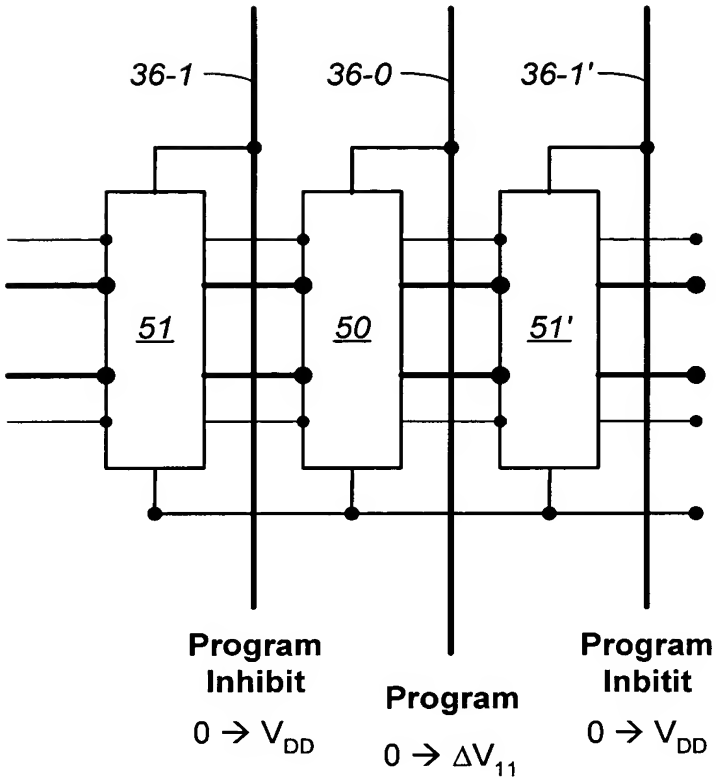
36-1
36-0
36-1'
51
50
51'
Program Inhibit
0 → V_{DD}
Program
0 → ΔV_{11}
Program Inbitit
0 → V_{DD}

FIG. 7A

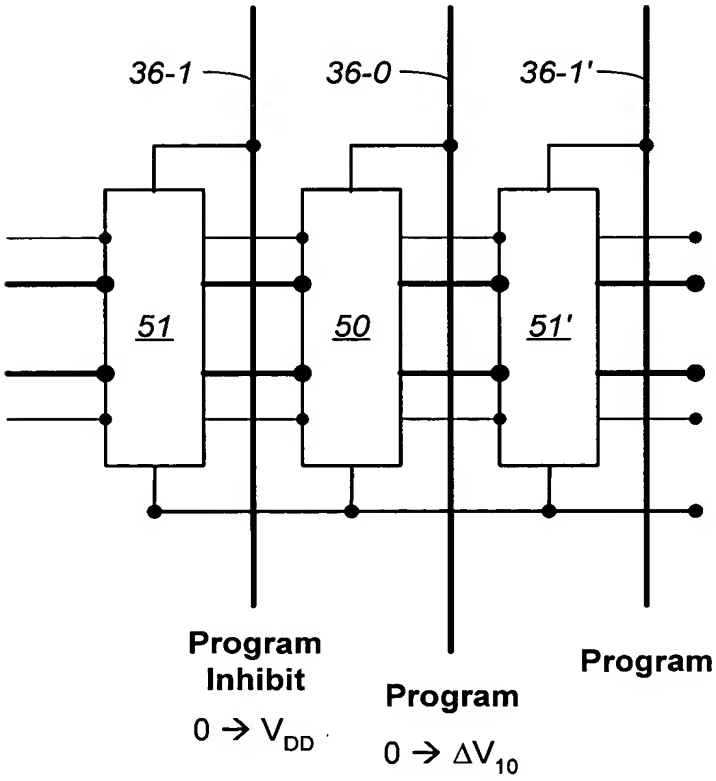
36-1
36-0
36-1'
51
50
51'
Program Inhibit
0 → V_{DD}
Program
0 → ΔV_{10}
Program

FIG. 7B

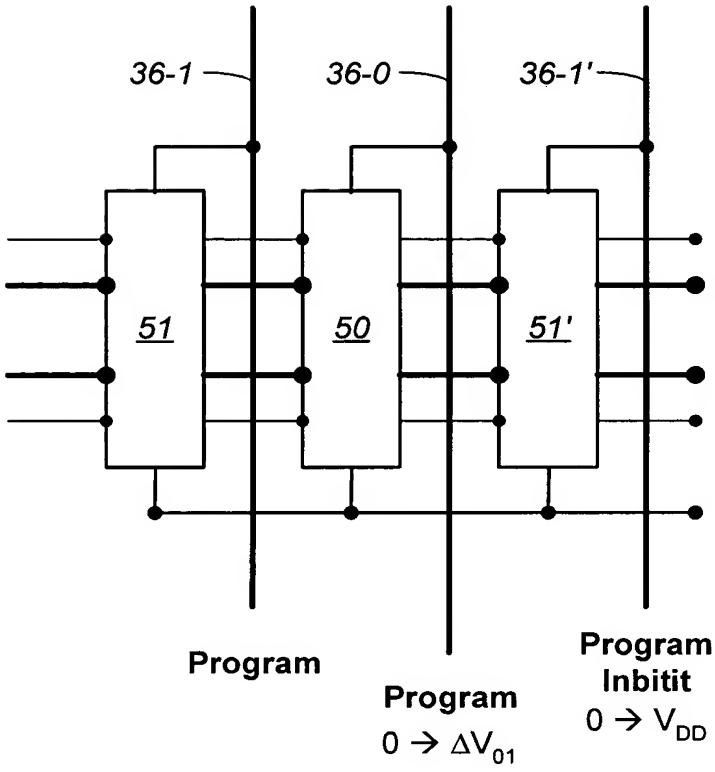
36-1
36-0
36-1'
51
50
51'
Program
Program
$0 \rightarrow \Delta V_{01}$
Program
Inbitit
$0 \rightarrow V_{DD}$

FIG. 7C

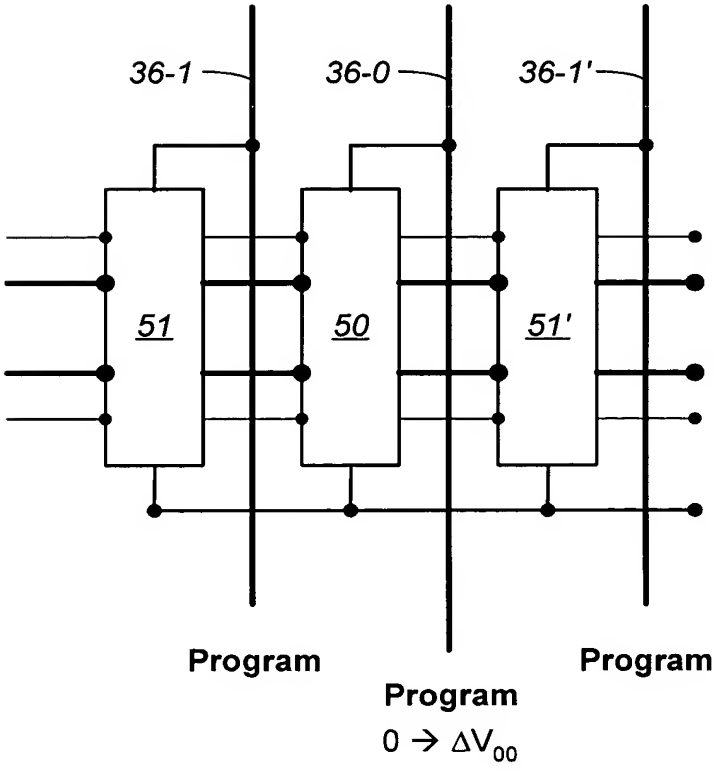
36-1
36-0
36-1'
51
50
51'
Program
Program
$0 \rightarrow \Delta V_{00}$
Program

FIG. 7D

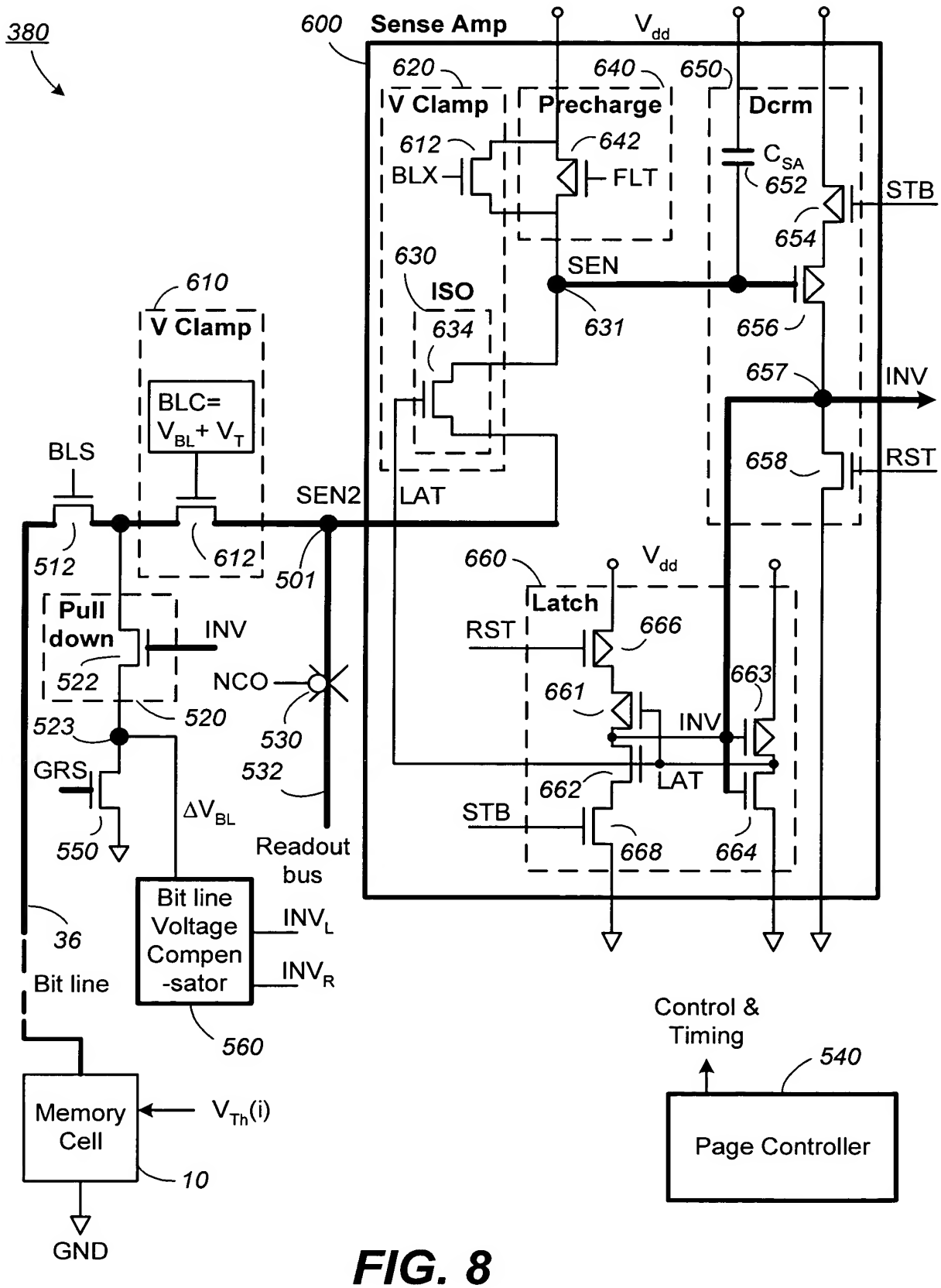
380
600
Sense Amp
V_{dd}
620
V Clamp
640
Precharge
650
Dcrm
612
BLX
642
FLT
C_{SA}
652
STB
654
630
ISO
634
SEN
631
656
610
V Clamp
BLC=
$V_{BL}+V_T$
657
INV
BLS
658
RST
SEN2
LAT
512
612
501
660
V_{dd}
Latch
Pull
down
INV
RST
666
522
NCO
661
663
520
523
530
INV
532
LAT
GRS
662
ΔV_{BL}
STB
550
668
664
Readout
bus
Bit line
Voltage
Compen
-sator
INV_L
INV_R
36
Bit line
560
Control &
Timing
540
Memory
Cell
$V_{Th}(i)$
Page Controller
10
GND

FIG. 8

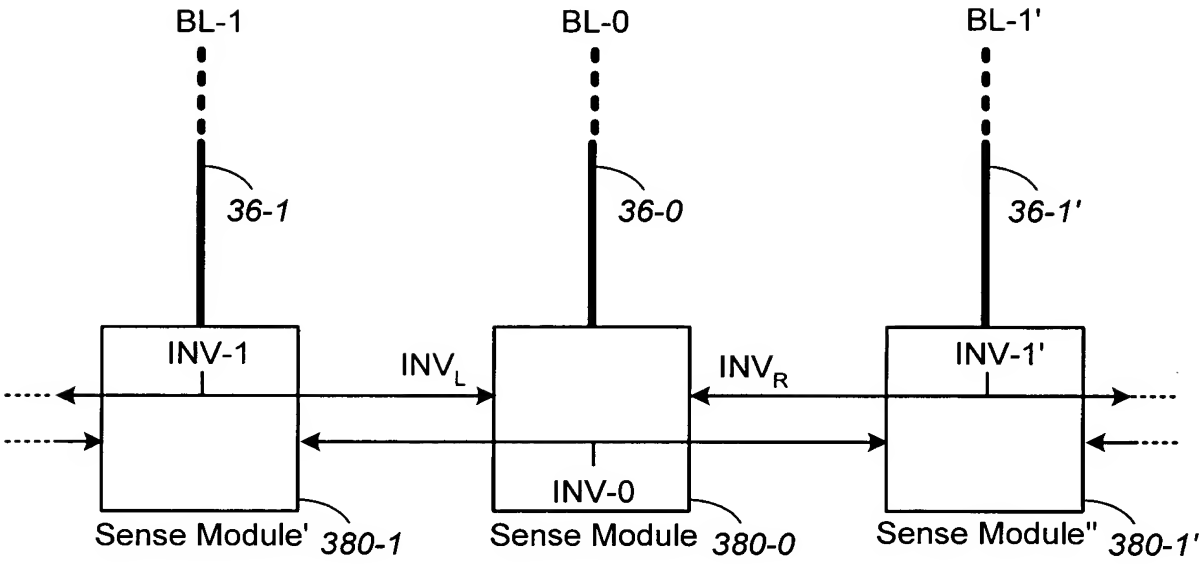
BL-1
BL-0
BL-1'
36-1
36-0
36-1'
INV-1
INV$_L$
INV$_R$
INV-1'
INV-0
Sense Module' 380-1
Sense Module 380-0
Sense Module" 380-1'

FIG. 9

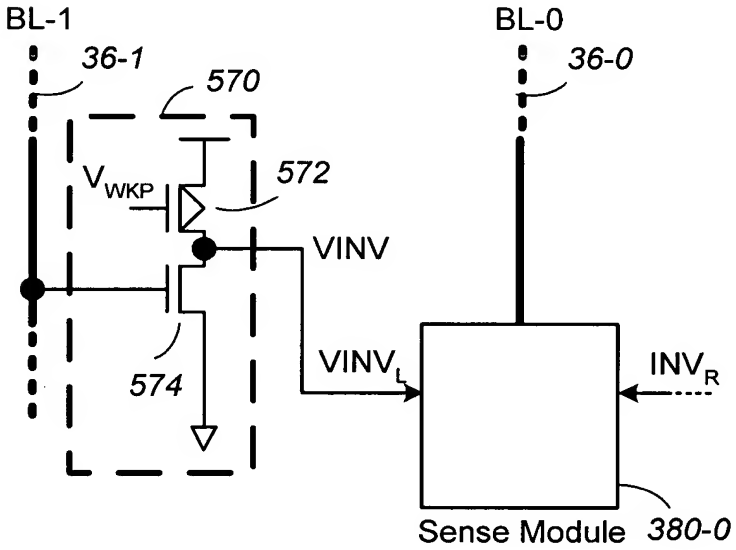
BL-1
BL-0
36-1
570
36-0
572
V_{WKP}
VINV
574
VINV$_L$
INV$_R$
Sense Module 380-0

FIG. 10

LEFT NEIGHBOR			Programming Storage Unit	RIGHT NEIGHBOR		
MODE	INV_L	V_{BL-1}	Bit line Offset ΔV_{BL-0}	MODE	INV_R	$V_{BL-1'}$
Program Inhibit	LOW	V_{DD}	ΔV_{11} (e.g., 0.3V)	Program Inhibit	LOW	V_{DD}
Program Inhibit	LOW	V_{DD}	ΔV_{10} (e.g., 0.15V)	Program	HIGH	ΔV
Program	HIGH	ΔV	ΔV_{01} (e.g., 0.15V)	Program Inhibit	LOW	V_{DD}
Program	HIGH	ΔV	ΔV_{00} (e.g., 0V)	Program	HIGH	ΔV

FIG. 11

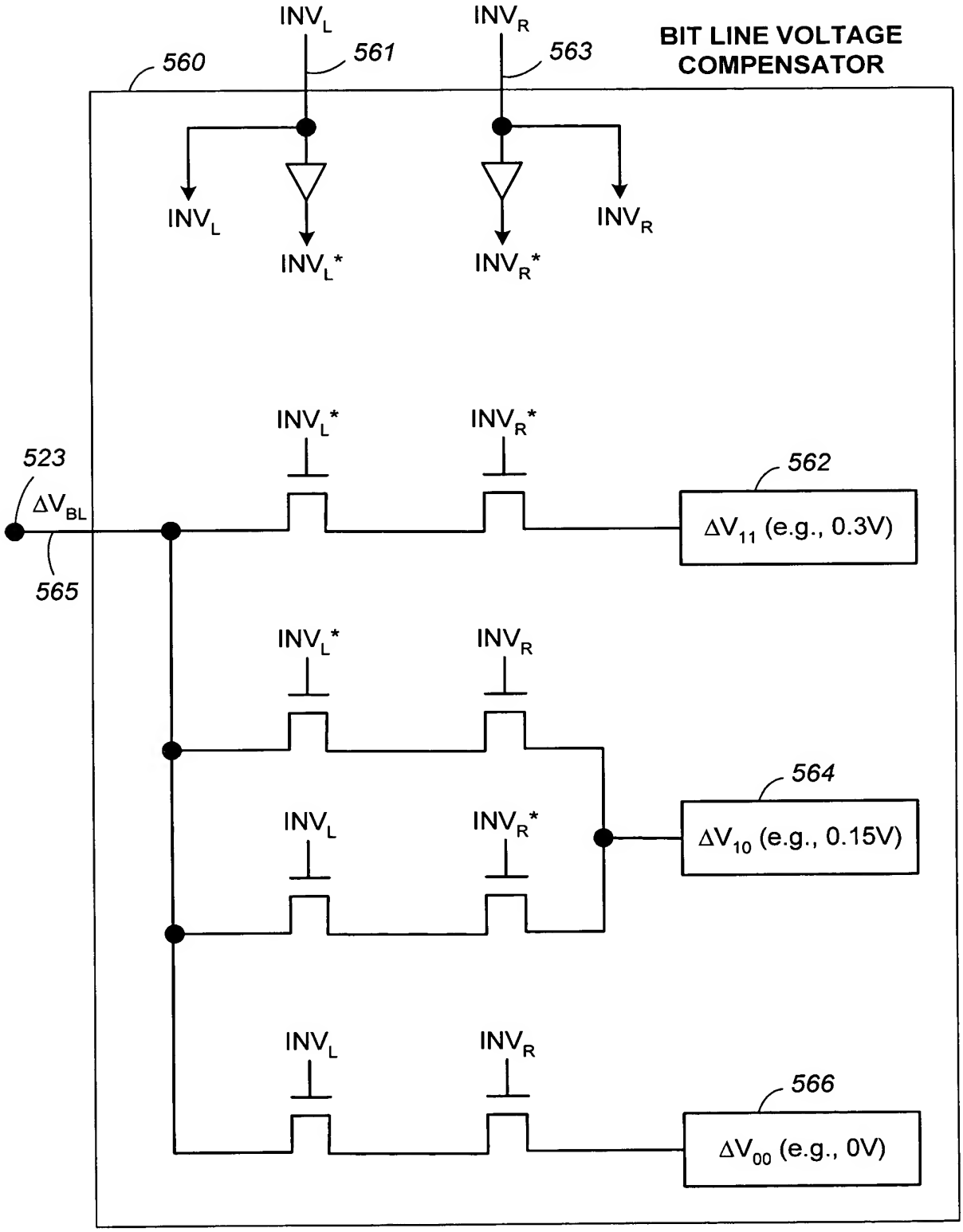
INV_L
INV_R
BIT LINE VOLTAGE COMPENSATOR
560
561
563
INV_L
INV_R
INV_L*
INV_R*
523
ΔV_BL
565
562
ΔV_11 (e.g., 0.3V)
564
ΔV_10 (e.g., 0.15V)
566
ΔV_00 (e.g., 0V)

FIG. 12

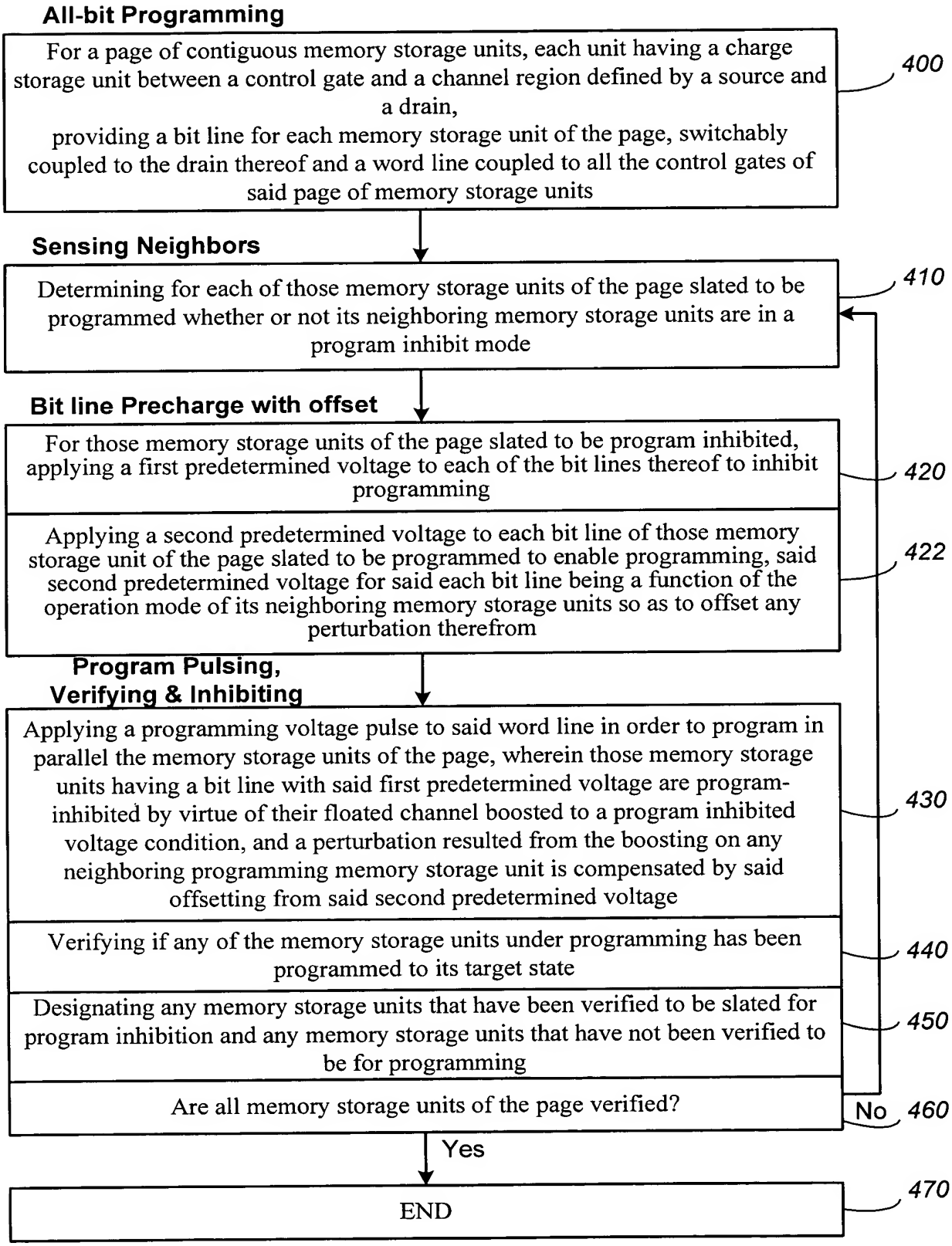
All-bit Programming
For a page of contiguous memory storage units, each unit having a charge storage unit between a control gate and a channel region defined by a source and a drain,
providing a bit line for each memory storage unit of the page, switchably coupled to the drain thereof and a word line coupled to all the control gates of said page of memory storage units
400
Sensing Neighbors
Determining for each of those memory storage units of the page slated to be programmed whether or not its neighboring memory storage units are in a program inhibit mode
410
Bit line Precharge with offset
For those memory storage units of the page slated to be program inhibited, applying a first predetermined voltage to each of the bit lines thereof to inhibit programming
420
Applying a second predetermined voltage to each bit line of those memory storage unit of the page slated to be programmed to enable programming, said second predetermined voltage for said each bit line being a function of the operation mode of its neighboring memory storage units so as to offset any perturbation therefrom
422
Program Pulsing, Verifying & Inhibiting
Applying a programming voltage pulse to said word line in order to program in parallel the memory storage units of the page, wherein those memory storage units having a bit line with said first predetermined voltage are program-inhibited by virtue of their floated channel boosted to a program inhibited voltage condition, and a perturbation resulted from the boosting on any neighboring programming memory storage unit is compensated by said offsetting from said second predetermined voltage
430
Verifying if any of the memory storage units under programming has been programmed to its target state
440
Designating any memory storage units that have been verified to be slated for program inhibition and any memory storage units that have not been verified to be for programming
450
Are all memory storage units of the page verified?
No
460
Yes
END
470

FIG. 13

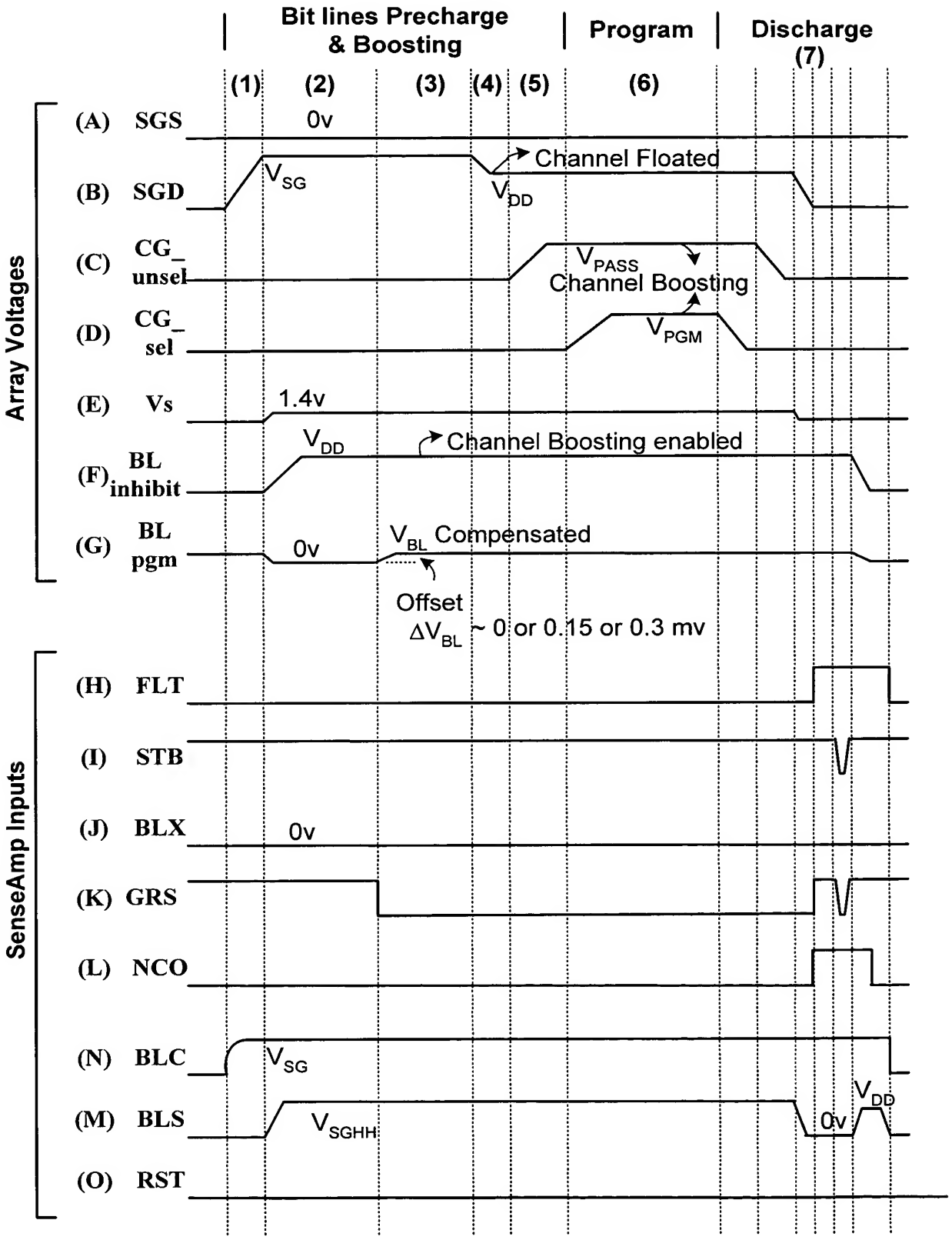
Bit lines Precharge & Boosting
Program
Discharge
(1)
(2)
(3)
(4)
(5)
(6)
(7)
Array Voltages
(A) SGS
0v
(B) SGD
V_{SG}
Channel Floated
V_{DD}
(C) CG_ unsel
V_{PASS}
Channel Boosting
(D) CG_ sel
V_{PGM}
(E) Vs
1.4v
(F) BL inhibit
V_{DD}
Channel Boosting enabled
(G) BL pgm
0v
V_{BL} Compensated
Offset
ΔV_{BL} ~ 0 or 0.15 or 0.3 mv
SenseAmp Inputs
(H) FLT
(I) STB
(J) BLX
0v
(K) GRS
(L) NCO
(N) BLC
V_{SG}
(M) BLS
V_{SGHH}
V_{DD}
0v
(O) RST

FIG. 14